

2. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

3. General Specification

Item	Dimension	Unit
Number of Characters	20 characters x 4Lines	—
Module dimension	98.0 x 60.0 x 13.6(MAX)	mm
View area	77.0 x 25.2	mm
Active area	70.4 x 20.8	mm
Dot size	0.55 x 0.55	mm
Dot pitch	0.60 x 0.60	mm
Character size	2.95 x 4.75	mm
Character pitch	3.55 x 5.35	mm
LCD type	STN, Positive, Transflective, Yellow Green	
Duty	1/16	
View direction	6 o'clock	
Backlight Type	LED Yellow Green	

4. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	°C
Storage Temperature	T_{ST}	-30	—	+80	°C
Input Voltage	V_I	V_{SS}	—	V_{DD}	V
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-0.3	—	7	V
Supply Voltage For LCD	$V_{DD}-V_0$	-0.3	—	13	V

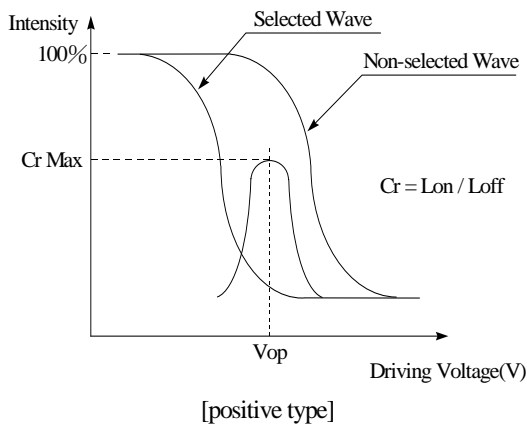
5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	—	4.5	5.0	5.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=-20^{\circ}\text{C}$	—	—	5.3	V
		$T_a=25^{\circ}\text{C}$	—	4.5	—	V
		$T_a=70^{\circ}\text{C}$	3.8	—	—	V
Input High Volt.	V_{IH}	—	$0.7 V_{DD}$	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	V_{SS}	—	0.6	V
Output High Volt.	V_{OH}	—	3.9	—	—	V
Output Low Volt.	V_{OL}	—	—	—	0.4	V
Supply Current	I_{DD}	$V_{DD}=5.0\text{V}$	1.0	1.2	1.5	mA

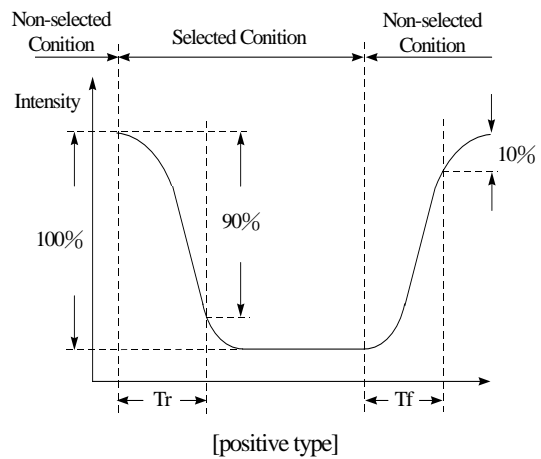
6. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ	$CR \geq 2$	20	—	40	deg
	(H) φ	$CR \geq 2$	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	150	200	ms
	T fall	—	—	150	200	ms

Definition of Operation Voltage (Vop)



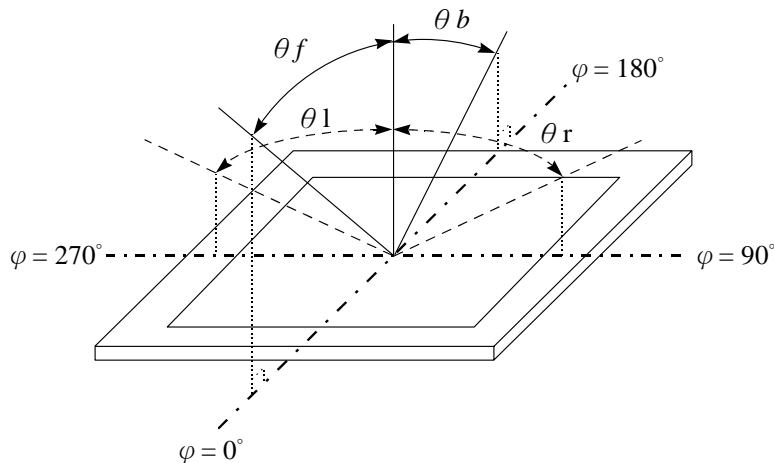
Definition of Response Time (Tr, Tf)



Conditions :

Operating Voltage : Vop Viewing Angle(θ , φ) : 0° , 0°
 Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

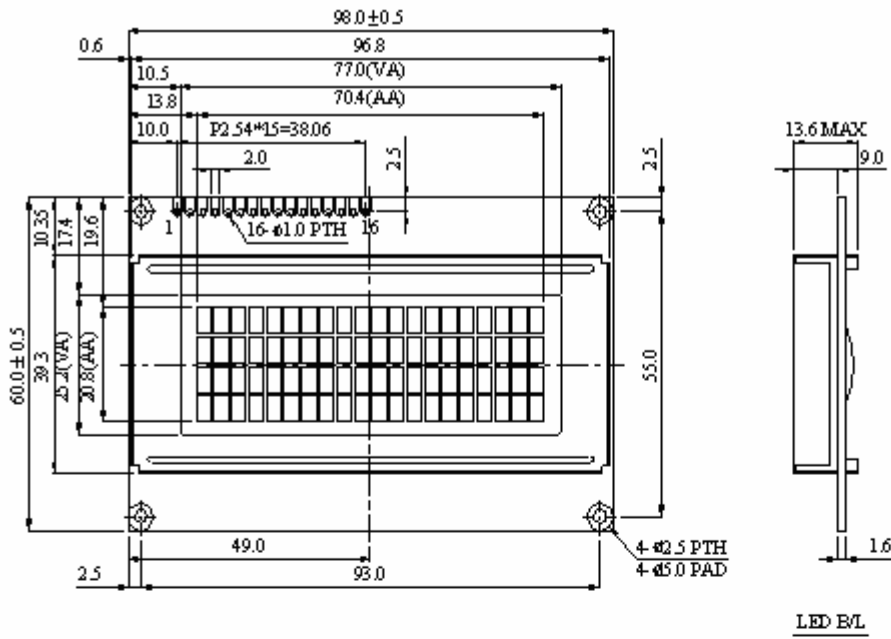
Definition of viewing angle($CR \geq 2$)



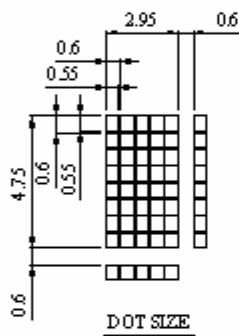
7. Interface Pin Function

Pin No.	Symbol	Level	Description
1	V _{SS}	0V	Ground
2	V _{DD}	5.0V	Supply Voltage for logic
3	VO	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bus line
8	DB1	H/L	Data bus line
9	DB2	H/L	Data bus line
10	DB3	H/L	Data bus line
11	DB4	H/L	Data bus line
12	DB5	H/L	Data bus line
13	DB6	H/L	Data bus line
14	DB7	H/L	Data bus line
15	A	—	LED +
16	K	—	LED -

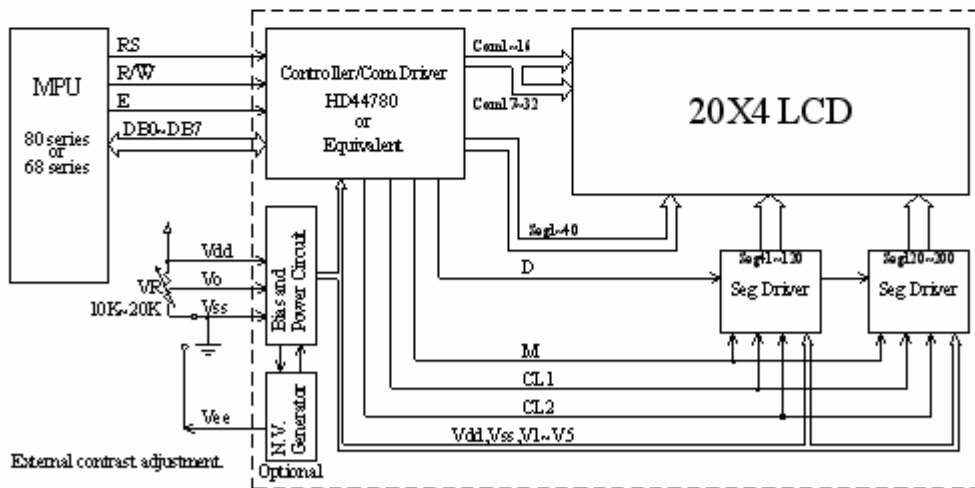
8. Contour Drawing & Block Diagram



Pin No.	Symbol
1	V _{SS}
2	V _{DD}
3	V _O
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A
16	K



The non-specified tolerance of dimension is ±0.3mm



Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
DDRAM address	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
DDRAM address	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

9. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

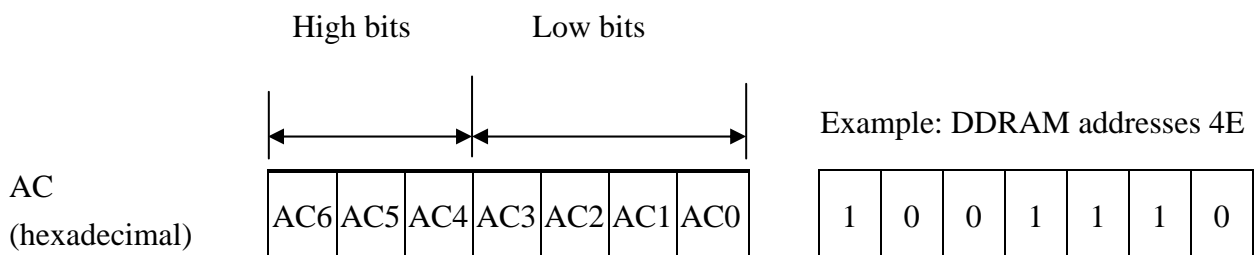
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80x8 bits or 80 characters. Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.



Display position DDRAM address

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

4-Line by 20-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

Table 1.

For 5 * 8 dot character patterns

Character Codes (DDRAM data)								CGRAM Address						Character Patterns (CGRAM data)												
7	6	5	4	3	2	1	0	5			4			3			2			1			0			
High				Low				High			Low			High				Low								
0 0 0 0 * 0 0 0								0 0 0						0 0 0	*	*	*	0				0				Character pattern(1)
														0 0 1	*	*	*	0	0	0	0					
														0 1 0	*	*	*	0	0	0	0					
														0 1 1	*	*	*	0	0	0	0					
														1 0 0	*	*	*	0	0	0	0					
														1 0 1	*	*	*	0	0	0	0					
														1 1 0	*	*	*	0	0	0	0					
														1 1 1	*	*	*	0	0	0	0					
														0 0 0	*	*	*	0	0	0	0					
														0 0 1	*	*	*	0	0	0	0					
0 0 0 0 * 0 0 1								0 0 1						0 1 0	*	*	*	0				0				Character pattern(2)
														0 1 1	*	*	*	0	0	0						
														1 0 0	*	*	*	0	0	0						
														1 0 1	*	*	*	0	0	0						
														1 1 0	*	*	*	0	0	0				Cursor pattern		
														1 1 1	*	*	*	0	0	0						
														0 0 0	*	*	*	0	0	0						
														0 0 1	*	*	*	0	0	0						
0 0 0 0 * 1 1 1								1 1 1						1 0 0	*	*	*	0				0				Cursor pattern
														1 0 1	*	*	*	0				0				
														1 1 0	*	*	*	0				0				
														1 1 1	*	*	*	0				0				

For 5 * 10 dot character patterns

Character Codes (DDRAM data)								CGRAM Address						Character Patterns (CGRAM data)																
7	6	5	4	3	2	1	0	5			4			3			2			1			0							
High				Low				High			Low			High				Low												
0 0 0 0 * 0 0 0								0 0						0 0 0 0	*	*	*	0	0	0	0	0	0	0	0	0				Character pattern
														0 0 0 1	*	*	*	0	0	0	0	0	0							
														0 0 1 0	*	*	*	0	0	0	0	0								
														0 0 1 1	*	*	*	0	0	0	0									
														0 1 0 0	*	*	*	0	0	0	0									
														0 1 0 1	*	*	*	0	0	0	0									
														0 1 1 0	*	*	*	0	0	0	0									
														0 1 1 1	*	*	*	0	0	0	0									
														1 0 0 0	*	*	*	0	0	0	0									
														1 0 0 1	*	*	*	0	0	0	0									
														1 0 1 0	*	*	*	0	0	0	0	0	0	0				Cursor pattern		
														1 0 1 0	*	*	*	0				0								
														1 1 1 1	*	*	*	*	*	*	*	*	*	*	*	*	*			
														1 1 1 1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*

■ : " High "

10.Character Generator ROM Pattern

Table.2

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)	!	"	#	\$	%	&	'	()	*	+	,	-	.	:
LLLH	CG RAM (2)	;	<	=	>	?	@	A	B	C	D	E	F	G	H	I
LLHL	CG RAM (3)	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X
LLHH	CG RAM (4)	Y	Z	[]	^	_	`	a	b	c	d	e	f	g	h
LHLL	CG RAM (5)	i	j	k	l	m	n	o	p	q	r	s	t	u	v	w
LHLH	CG RAM (6)	x	y	z	{	}	~	!	"	#	\$	%	&	'	()
LHHL	CG RAM (7)	*	+	,	-	.	:	;	<	=	>	?	@	A	B	C
LHHH	CG RAM (8)	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R
HLLL	CG RAM (1)	S	T	U	V	W	X	Y	Z	[]	^	_	`	a	b
HLLH	CG RAM (2)	c	d	e	f	g	h	i	j	k	l	m	n	o	p	q
HLHL	CG RAM (3)	r	s	t	u	v	w	x	y	z	{	}	~	!	"	#
HLHH	CG RAM (4)	\$	%	&	'	()	*	+	,	-	.	:	;	<	=
HHLL	CG RAM (5)	>	?	@	A	B	C	D	E	F	G	H	I	J	K	L
HHLH	CG RAM (6)	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	[
HHHL	CG RAM (7)]	^	_	`	a	b	c	d	e	f	g	h	i	j	k
HHHH	CG RAM (8)	l	m	n	o	p	q	r	s	t	u	v	w	x	y	z

11. Instruction Table

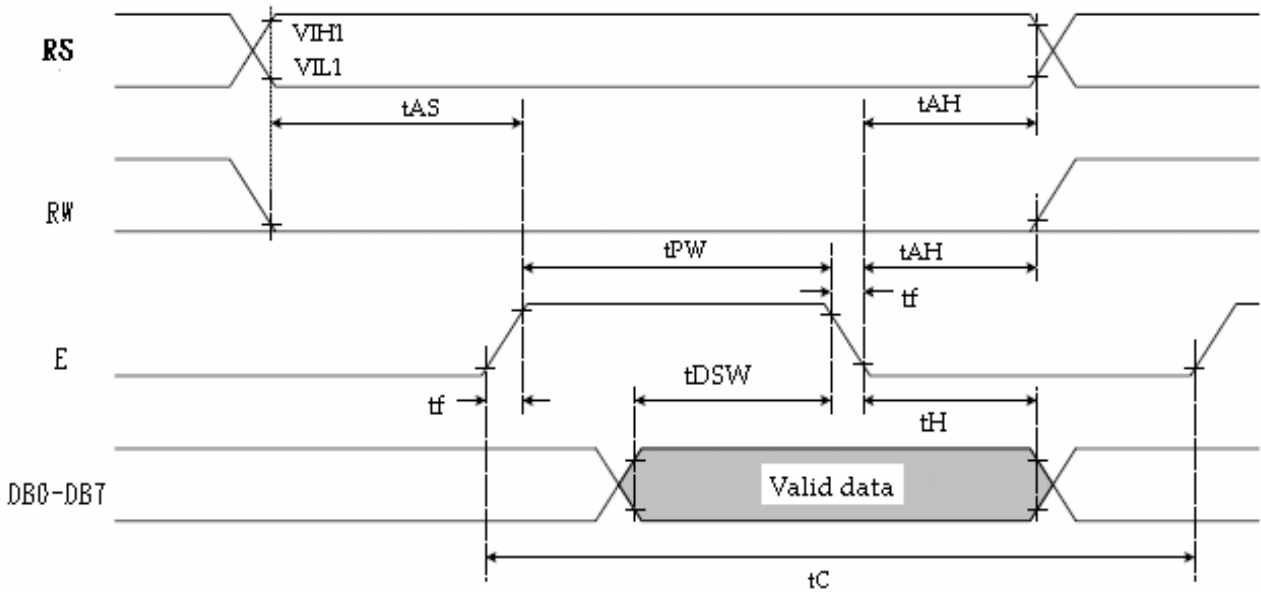
Instruction	Instruction Code										Description	Execution time (fosc=270Khz)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	—	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	—	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	—	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	—	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	—	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	—	Read data from internal RAM (DDRAM/CGRAM).	43 μs

* "—" : don't care

12. Timing Characteristics

12.1 Write Operation

- Writing data from MPU

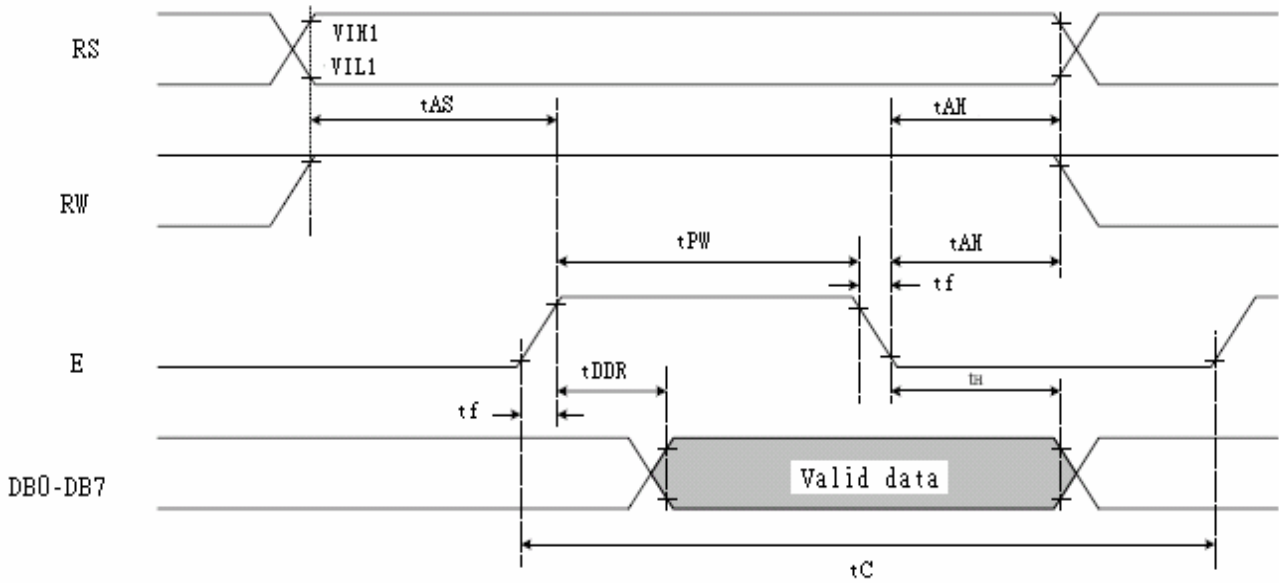


Ta=25°C, VDD=5.0V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	T _C	1200	—	—	ns
Enable pulse width	T _{PW}	140	—	—	ns
Enable rise/fall time	T _R , T _F	—	—	25	ns
Address set-up time (RS, R/W to E)	t _{AS}	0	—	—	ns
Address hold time	t _{AH}	10	—	—	ns
Data set-up time	t _{DSW}	40	—	—	ns
Data hold time	t _H	10	—	—	ns

12.2 Read Operation

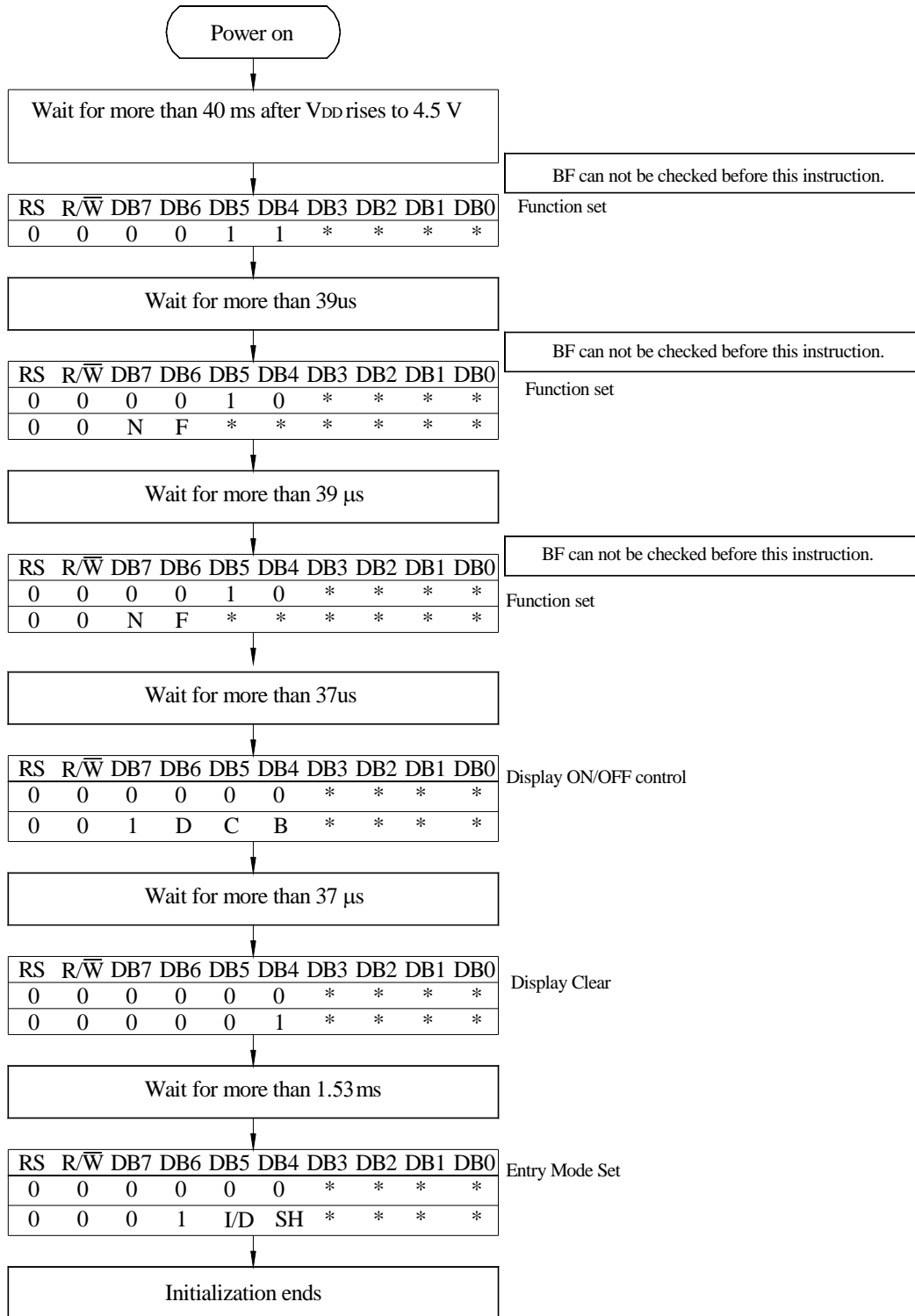
- Reading data from ST7066U



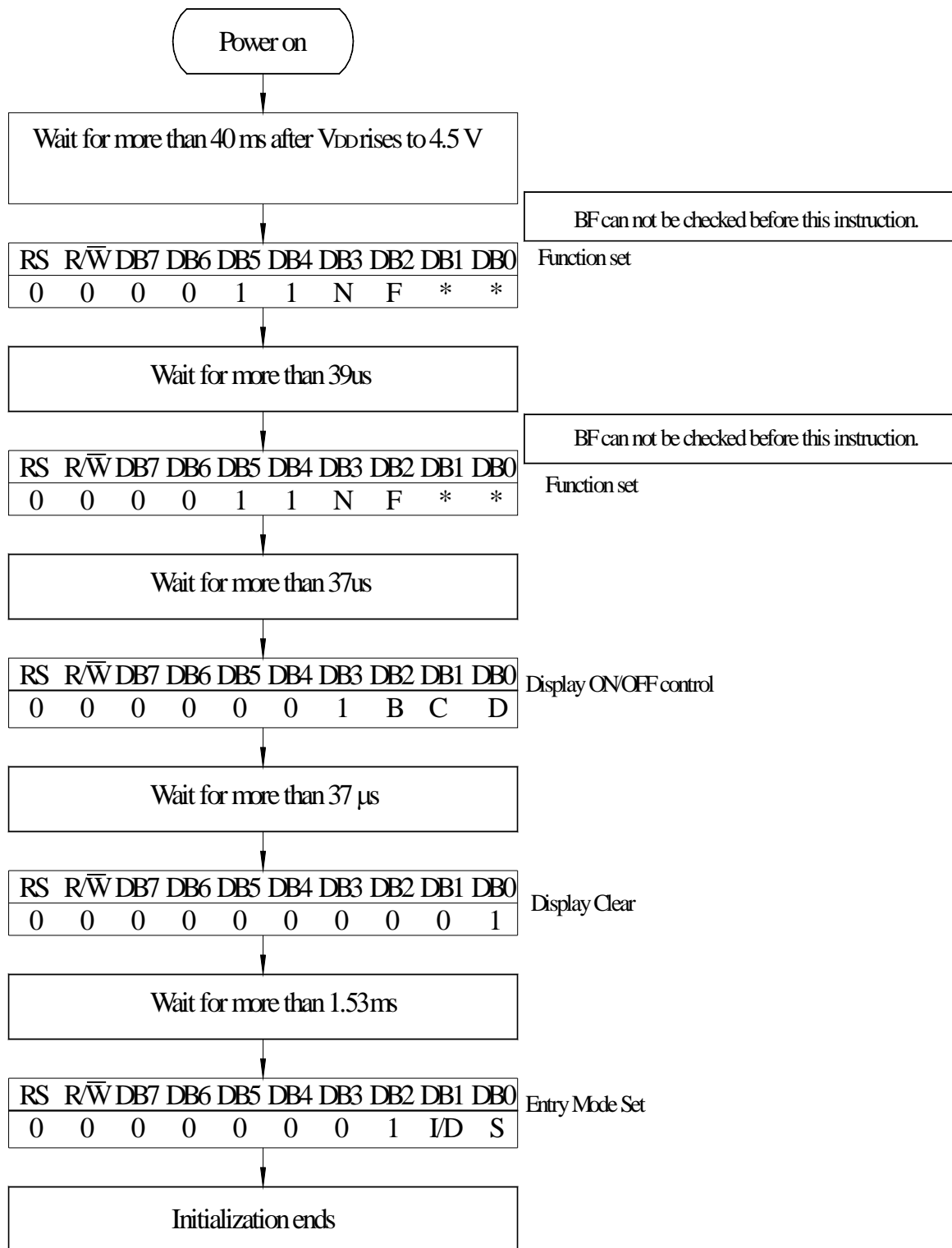
Ta=25°C, VDD=5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	T _C	1200	—	—	ns
Enable pulse width (high level)	T _{PW}	140	—	—	ns
Enable rise/fall time	T _R , T _F	—	—	25	ns
Address set-up time (RS, R/W to E)	t _{AS}	0	—	—	ns
Address hold time	t _{AH}	10	—	—	ns
Data delay time	t _{DDR}	—	—	100	ns
Data hold time	t _H	10	—	—	ns

13. Initializing of LCM



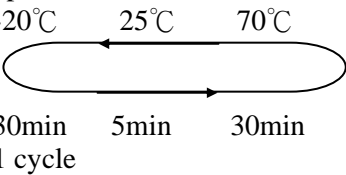
4-Bit Ineterface



8-Bit Inerface

14. Reliability

Content of Reliability Test (wide temperature, -20°C~70°C)

Environmental Test			
Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80°C 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 200hrs	—
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60 °C, 90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60°C, 90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation  30min 5min 30min 1 cycle	-20°C/70°C 10 cycles	—
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V, RS=1.5kΩ CS=100pF 1 time	—

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.

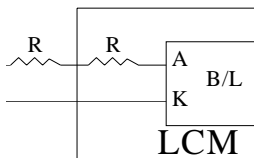
15.Backlight Information

Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	I _{LED}	224	280	420	mA	V=4.2V
Supply Voltage	V	4.0	4.2	4.4	V	—
Reverse Voltage	V _R	—	—	10	V	—
Luminous Intensity	I _V	—	180	—	CD/M ²	I _{LED} =280mA
Wave Length	λ _p	—	570	—	nm	I _{LED} =280mA
Life Time	—	—	100000	—	Hr.	I _{LED} ≤ 280mA
Color	Yellow Green					

Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).

2.Drive from pin15,pin16



ill never get Vee output from pin15)